10 Sep 1992

TS3NM-B

TEST SET, LOGIC

1. GENERAL. This procurement requires a self-contained, solid-state logic troubleshooting kit capable of detecting and analyzing in-circuit logic failures. The kit shall be able to inject pulses into logic circuitry and monitor the level transitions. The kit shall consist of a logic probe, logic pulser, and a dual-in-line package (DIP) monitor clip.

2. CLASSIFICATION. Type II, Class 5, Style EP, and Color R in accordance with MIL-T-28800 except nominal power source requirements are not invoked.

3. OPERATIONAL REQUIREMENTS. The probe, pulser, and monitor clip shall be capable of in-circuit logic level analysis of transistor-transistor logic (TTL) and complementary metal oxide semiconductor (CMOS) logic within the minimum ranges and accuracies specified below.

3.1 Logic probe.

3.1.1 TTL logic levels.

a. Logic one: 1.8 to 2.4 volts peak.

b. Logic zero: 0.4 to 1 volt peak.

3.1.2 CMOS logic levels.

3.1.2.1 3 to 10 Vdc supply.

a. Logic one: (0.7 X supply voltage) ±0.5V

b. Logic zero: (0.3 X supply voltage) ±0.5V

3.1.2.2 10 to 18 Vdc supply.

a. Logic one: (0.7 X supply voltage) ±1V

b. Logic zero: (0.3 X supply voltage) ±1V

3.1.3 Probe pulse width. Minimum detectable pulse width: 10 ns or less. A pulse-stretching feature shall be provided to cause a flashing light during pulse activity.

3.1.4 Pulse repetition frequency limit. 80 MHz for TTL and 40 MHz for CMOS.

3.1.5 Probe impedance. 25 kilohms minimum.

3.1.6 Probe display. The logic probe display shall be capable of indicating the following conditions via a light:

a. Normal logic levels (HI-LOW).

b. Pulse activity.

c. Open and short circuits.

d. Excessive and inadequate levels.

3.1.7 Probe overload protection. 120V continuous from dc to 1 kHz.

3.1.8 Power. The logic probe shall be powered by the circuit under test. Overvoltage protection: ±25 Vdc for 1 minute.

3.2 Logic pulser. The pulser shall automatically drive circuits connected to it to their opposite state. Operational parameters shall be as detailed below.

3.2.1 Output current. 0.65A for TTL and 0.1A for CMOS.

3.2.2 Pulse width. 0.5 us for TTL and 5 us for CMOS.

3.2.3 Pulse voltages. TTL: high - 3V or greater, low - 0.8V or less. CMOS: high - supply voltage minus 1 Vdc or greater, low - 0.5V or less.

3.2.4 Pulser impedance. Less than 2 ohms when active and more than 1 megohm when off.

3.2.5 Pulser power. The logic pulser shall be powered by the circuit under test. Overvoltage protection: ±25 Vdc for 1 minute.

3.3 Logic clip. The logic clip shall be compatible with DIP integrated circuits of up to 16 pins and have a state indicator for each pin.

3.3.1 Input. Turn-on threshold: (0.4 ±0.06 Vdc) X supply voltage or greater for logic high indication.

3.3.2 Clip overload protection. 30 Vdc for one minute.

4. GENERAL REQUIREMENTS.

4.1 Power source. The clip shall be powered by the DIP under test that provides 4 to 18 Vdc across any two pins.

4.2 Weight. 1.4 kg (3 lb) maximum.

4.3 Lithium batteries. Per MIL-T-28800, lithium batteries are prohibited without prior authorization. Requests for approving the use of lithium batteries, including those encapsulated in integrated circuits, shall be submitted to the procuring activity at the time of submission of proposals. Approval shall apply only to the specific model proposed.